In the Drawings

In FIG. 1, a CLK signal is added to the phase error quantizer 110.

In FIG. 5, the label of "CLK" is added to the CK input terminal of the flip-flop in the reset unit 420.

Attachments

Replacement Sheets

REMARKS

The Examiner is thanked for the thorough examination of the present application. The Office Action, however, tentatively rejected all claims 1-17.

In the Drawings

FIGs. 1 and 5 are amended herein to make certain cosmetic changes. In FIG. 1, a clock signal CLK is added going into the phase error quantizer 110. Further, in Fig. 5, the label of "CLK" is added going into the CK input terminal of the flip-flop in the reset unit 420. Applicant notes that the CLK signal added in Fig. 1 is the same clock signal that is illustrated in Fig. 5, Fig. 7, and Fig. 8. The amendments to the drawings are well supported by the detailed description as originally filed, including paragraph [0005] of the background section, which states: "[w]hen the phase error between the input signal Fr and the feedback signal Fi is smaller than a clock signal, the quantizer cannot detect the phase error therebetween and thus is not able to obtain a count signal COUNT", and paragraph [0020] of the detailed description section, which states: "[t]he reset unit 420 is a D-type flip-flop ... receives a clock signal CLK at a clock input terminal CK ... the clock signal CLK herein in this embodiment adopts the same clock signal as is used for triggering purpose in the post-stage quantizer." Accordingly, these drawing amendments add no new matter to the application.

Rejections under 112, second paragraph:

The Office Action rejected claims 2, 7, 9, and 12 under 35 U.S.C. § 112, second paragraph as allegedly indefinite. This rejection is premised on the belief that no embodiment is seen in any of the drawing figures or in any portion of the specification where the first reset signal is used for resetting both the phase error detector and also the phase error judgment unit. Applicant respectfully submits that in at least one embodiment (e.g., in Fig. 5) the signal used for resetting the phase error judgment unit (*i.e.*, the second reset signal) is actually an inverted version of the first reset signal, which is used for resetting the phase error detector. Such a disclosure fully supports the limitation "that the phase error judgment unit is reset ***according*** to the first reset signal," since the reset of the phase error judgment unit is in effect dependent of the value of the first reset signal, at least in some embodiments. The mention of an alternative implementation, where "the phase error judgment unit 410 may also be reset by the first reset signal RESET1 via an inverter" (in paragraph [0020]) also supports this claim language. Accordingly, the rejection of claims 2 and 12 should be withdrawn.

Claims 7 and 9 were rejected for filing to provide proper antecedent support for the claimed third and fourth flip-flops. Applicant does not believe this is a proper rejection, as there is no requirement that labels like "third" and "fourth" be used ONLY after using labels of "first" and "second." In this regard, the terms are merely labels. The choice of naming of elements in claims is of trivial significance, as long as it can serve to distinguish among various components as described and as claimed. In the underlying case the choice of naming makes perfect sense since it echoes the naming convention in the detailed

description. Moreover, even though claim 7 depends from claim 1, the undersigned submits that using labels of "first" and "second" would result in confusion over the use of the same terms in claim 6. That is, both claims 6 and 7 would reference "first" and "second" flip-flops, and the "first" flip-flop of claim 6 would refer to a different flip-flop than the "first" flip-flop of claim 7. Based on claim interpretation tenants (including the Doctrine of Claim Differentiation), Applicant submits that changing the labels of "third" and "fourth" in claim 7 to "first" and "second" would create problems, and therefore, Applicant has declined to make this change.

Objection under 37 CFR 1.83(a):

The Office Action objected to the drawings. Applicant submits that this objection has been rendered moot by the amendments made to the drawings herein.

Rejection under 102 and 103:

The Office Action rejected claims 1-10 under 35 U.S.C. § 102(e) as allegedly anticipated by Chou (US 7,102,448). The Office Action also rejected claims 11-17 under 35 U.S.C. § 103(a) as allegedly unpatentable over Chou. First of all, the Applicant would like to point out that Chou et al. is not a "prior art" falling under the definition of 35 USC 102(e), or any other subsection of section 102. In this regard, that the present application has a filing date of April 7, 2004, with a foreign priority date of May 6, 2003. However, Chou et al. Has a U.S. filing date of March 31, 2004. Although Chou has an earlier foreign priority date of April 8, 2003, such a priority date is not effective to constitute prior art to the present application. *See e.g., In re Hilmer*, 424 F.2d 1108 (CCPA 1970).

Therefore, the rejections of claims 1-17 based on Chou should be withdrawn.

The Office Action also rejected claims 1, 4, and 5 under 35 U.S.C. § 102(e) as allegedly anticipated by Yoo (US 6,683,478). Applicant respectfully requests reconsideration and withdrawal of this rejection.

As amended herein, independent claim 1 recites:

> 1. A phase frequency detector comprising:
> a phase error detector outputting a phase error signal according to a first input signal and a second input signal;
> a phase error judgment unit outputting a phase error judgment signal according to the first input signal and the second input signal; and
> ***a reset unit outputting a first reset signal according to the phase error judgment signal and receiving a clock signal, the first reset signal resetting the phase error detector, wherein the outputting of the first reset signal is triggered by the clock signal.***

(*Emphasis added.*) Claim 1 patently defines over the cited art for at least the reason that the cited art fails to disclose the features emphasized above.

In contrast to the claimed embodiments, Yoo discloses a phase detector 100 used in a delay locked loop (DLL) as shown in Fig. 1. The goal of Yoo is "to provide a phase detector system and method which operate correctly, regardless of the point of time at which the operation of delay locked loop is initialized with respect to the phases of the reference and feedback clock signals." (see column 4, line 53-57 of Yoo) This is significantly different than an object of the present application, which, in one respect, aims to account for the "dead zone" phenomenon encountered in a digital phase locked loop (PLL) system when the phase error between the input signal Fr and the feedback signal Fi becomes too small and as a result becomes invisible as opposed to the resolution of the clock signal adopted in subsequent component, such as the phase error quantizer 110.

Reflecting such a difference, claim 1 (as amended) defines outputting of the first reset signal by the reset unit is triggered by a clock signal. It is the adoption of a clocked reset signal generation scheme in the embodiments of the present application that enables a proper delay in the reset of the phase error detector, and consequently the desired detection of the phase error by the phase error quantizer. In contrast, Yoo fails to teach resetting the flip-flops 110 and 120 based on triggering of any clock signal. Indeed, Yoo doesn't even seek to account for the "dead zone" phenomenon as otherwise properly resolved by embodiments of the present application.

For at least this reason, independent claim 1 (as amended) patently defines over Yoo. As claims 2-10 depend from claim 1, these claims define over Yoo for at least the same reasons.

Independent claim 11 has also been amended herein to recite:

> 11. A phase locked loop, comprising:
> a phase frequency detector outputting a phase error signal according to a first input signal and a second input signal;
> a quantizer outputting a count signal according to the phase error signal; and
> an oscillator generating the second input signal according to the count signal;
> wherein the phase frequency detector comprises:
> a phase error detector outputting the phase error signal according to the first input signal and the second input signal;
> a phase error judgment unit outputting a phase error judgment signal according to the first input signal and the second input signal; and
> ***a reset unit outputting a first reset signal according to the phase error judgment signal, the first reset signal resetting the phase error detector, wherein the quantizer is triggered by a clock signal, and the reset unit is also triggered by the clock signal***.

(*Emphasis added*.) Claim 11 patently defines over the cited art for at least the reason that the cited art fails to disclose the features emphasized above.

In short, the features emphasized above are similar, in relevant respect, to the defining features of claim 1. Consequently, claim 11 defines over Yoo for the same reasons set for the above in connection with claim 1. As claims 12-17 depend from claim 11, the rejections of these claims should be withdrawn for at least the same reasons.

New claims:

New independent claim 18 is introduced, which incorporates the claim limitation of the reset unit generating a second reset signal for resetting the phase error judgment unit. New independent claim 19 is also introduced, which incorporates the claim limitation of a third flip-flop receiving the first input signal and a fourth flip-flop receiving the second input signal in the phase error judgment unit. These features, in combination with the remaining features, patently define over the cited art.

The Lo and Katayama references:

On page 7, the Official Action stated that Fig. 2 of Katayama (US 5,896,066) and Fig. 1A of Lo (US 6,140,853) is believed to anticipate claim 1. Applicant respectfully disagrees. First, Applicants submits that the amendment to claim 1 renders this application of Katayam and Lo moot.

In addition, the Office Action has failed to properly apply the cited references against the claims. In this regard, Applicant notes that the rejection fails to comply with the requirements specified by the MPEP. Specifically, the MPEP states "Where a claim is rejected for any reason relating to the merits thereof if should be 'rejected' ***and the ground of rejection fully and clearly stated.***" MPEP § 707.07(d). Should the Examiner maintain

these rejections, Applicant respectfully requests that any ensuing Office Action provide a complete application of the cited art against the rejection claim(s).

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with this amendment and response. If, however, any fee is deemed to be payable, you are hereby authorized to charge any such fee to Deposit Account No. 20-0778.

Respectfully submitted,

/Daniel R. McClure/

By: _____

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